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Dynamic Voltage Rail Audio Amplifier

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Senior Design Final Report

Design Team #01

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Table of Contents

List of Tables

List of Figures

Abstract (EV)

The goal of this project is to create a high-quality, power-efficient audio amplifier. Most modern audio amplifiers use a constant amount of power regardless of the signal that is being amplified. This means that both loud and quiet portions of the audio signal require the same amount of power to amplify. The idea for this high-quality, power-efficient audio amplifier is that the quieter portions of the audio signal can be amplified using less power. This will be achieved by first analyzing the audio signal and controlling the power source based on the signal's needs. Therefore, louder parts of the audio signal will use the typical amount of power, while quieter parts of the signal will not use as much power. When comparing a standard audio amplifier and the high-quality power-efficient audio amplifier, the average power usage for the power-efficient amplifier should be less than the standard amplifier.

I. Problem Statement

Need Statement (TO, ST)

Music is a key part of every culture around the world and an important aspect in the lives of millions of people. In today's day and age, music is everywhere: in films, on our phones, on our computers, through the stereos in our cars and in our homes. Every aspect of life has been shaped in a way to accompany a means to play music. As the demand for quality music always seems to be increasing, the means to play music is directly increasing as well, and that means is through the use of power amplifiers and speakers. To drive these amplifiers and speakers, there is a need for a power source (typically a battery or the power available from an outlet). Generally, amplifiers use a fixed source voltage. However, if the input signal becomes quieter, the maximum available voltage (i.e., the fixed source voltage) is not needed and that power goes to waste. In order to have good linearity, audio components consume a lot of power in respect to

the conveniences that they offer and are therefore power inefficient. With this inefficiency, a lot of heat (wasted energy) is dissipated; to combat this, usually more output components are needed to combat the thermal dissipation and this in turn increases the price. [1] There is a need for a system which dynamically control the source voltage of an amplifier to eliminate wasted power. These are a few of many issues that audio amplifier designers come across in search for the perfect balance of efficiency, output audio signal quality and performance.

Objective Statement (AC, EV, TO)

In order to obtain higher power efficiency within the limits of a speaker's capabilities, the power usage of an audio amplifier may be designed to reflect parts of an audio signal that require more or less power. For example, a quieter portion of a song requires less output power whereas a louder portion of a song may require more output power. One way of combating this is to design an amplifier that can read an input signal, and then adjust the supply voltage of the output signal to best suit the needs utilizing the simple Power = Voltage x Current relationship. The amplifier should dually improve the quality of the output at low volumes by providing less noise alongside also decreasing the overall power usage when the input signal is smaller.

Background Information (AC, TO, ST, EV)

The senior design project at hand presents an idea to create an audio amplifier which is capable of tracking an input signal and using a time delay to analyze the input signal; the power input of the amplifier can then be adjusted in real time to track the instantaneous input signal amplitude; resulting in a higher power efficiency [2]. The main objective of this design is to amplify an audio input signal more power efficiently while still maintaining a high level of

4

quality. The present senior design team conducted preliminary research to find basic theory behind the proposed concept, current methods for implementing the proposed concept, limitations of current designs and technologies, similarities between the proposed concept and existing designs and technologies, along with existing and patented technologies that may be relevant to the proposed design. The research done on these topics will provide insight into the feasibility and potential of the project.

In rudiment, the theory for this project is to amplify an audio signal. Amplifiers are circuits/circuit-components that take an input signal, multiply the input signal by a scalar value, and then reproduce an output signal that is a scaled version of the input signal. There are multiple methods and devices that can be used for providing amplification. To further illustrate amplification, the focus will be on three-terminal devices called transistors. To achieve amplification using transistors, an input signal is applied to one of the three terminals of a transistor (e.g. a gate node of a metal-oxide-semiconductor field-effect transistor, hereinafter referred to as a MOSFET) and an output is then set to another terminal (e.g. a source node of the MOSFET). The chosen input and output terminals are generally dependent on two factors: the amount of gain the amplifier is required to apply to the input signal, and the signal manipulations desired at the output of the amplifier. By using multiple transistors, it is possible to created different types of amplifiers, each with different behavioral characteristics and parameters. At least two terminals in the transistor circuit are connected to upper and lower limit supply voltages, wherein resistors are typically used to bias the voltages and currents as needed. The two supply voltages serve as maximum and minimum possible voltage values for the amplified signal. An output signal that is to be amplified beyond one of the maximum or minimum possible voltage values will be "clipped". Clipping leads to distortion and noise which pollutes

the original input signal. It is important to understand every aspect of audio power amplification and how to combat the complications that arise [3]. In order to achieve better power efficiency, the amplifier will use digital signal processing to analyze the input signal and adjust the supply voltage to facilitate the output signal accordingly. This will be performed by using an embedded microcontroller such as a Microchip PIC series to sample incoming data. The microcontroller can then use a set of predetermined threshold voltages to determine the power requirements of the output. If the input signal voltage is large enough such that it attains a predetermined threshold voltage, the voltage supplied for the output will be increased. Likewise if the input signal voltage falls below a predetermined threshold voltage, the voltage supplied for the output will be decreased. It is to be noted that there may be multiple threshold "steps" that can lead to changes in voltage supplied for the output signal

Currently, there are many different classifications of amplifiers that are widely used in audio amplification. Each classification utilizes a different configuration of transistors and supply voltages. These classifications are typically denoted by uppercase letters including class A, B, C, D, G, H, etc. There also exist combinations of classes such as class AB and AB-D amplifiers. Each class has its own strengths and weaknesses. For example, class A amplifiers have high linearity (i.e., quality) but they are not power efficiency. Class B amplifiers provide high power efficiency with the tradeoff being that they provide weak signal quality. Combinations of classes, such as class AB amplifiers, can be arranged in such a way that the positive aspects of each of the classes given in the name are enhanced while the negative tradeoffs are suppressed. The characteristics of classes and combined classes vary in regards to linearity, power efficiency, conduction angle, and more. By combining different types of

transistors and amplification styles, different results can be achieved containing a wide range of characteristics associated with each amplification class.

Many present-day amplifiers are limited by having to choose between power efficiency and signal quality. Designing amplifiers is fundamentally a balancing act between these two limitations. As mentioned before, class A amplifiers can achieve a high signal linearity, but they have low power efficiency. Contrary to this, class B amplifiers are very efficient since their conduction angle is only 180 degrees (i.e., class A amplifiers conduct at 360 degrees allowing for high linearity, while class B amplifiers conduct at 180 degrees with distortion occurring at a zero-crossing point between positive and negative values of the amplified signal), but this is also the reason why they provide less linearity [4]. As Chambers writes in his entry about being an audiophile, it is very important to maintain both the utmost quality while still having complete control of the audio signal [5].

Audio amplifiers, including the proposed amplifier, are fundamentally similar across the board with the simple fact that each will take an input signal and output an amplified version of that input signal. The main differences are distinguished within the design work itself; primarily within the trade-offs designers are willing to make in order to achieve desired results. For this project, it is very important to maintain both quality and power efficiency at both high and low volumes. To accomplish this, envelope tracking (ET) will be used. According to "A review of envelope tracking power supply for mobile communication systems," by Xinbo Ruan, Yazhou Wang, and Qian Jin, "[t]he basic idea of the ET technique is to modulate the supply voltage of the linear power amplifier to track the envelope of the radio frequency signal, and thus, the drain efficiency of the linear power amplifier is improved." [6] This quote describes ET use for radio frequency signals; this project however, will apply the science behind ET to audio signals being

7

sent through an audio amplifier in an effort to perform power efficient amplification. The amplitude of the audio signal will be continuously tracked by a microcontroller, and the microcontroller will allow for the supply voltage to be adjusted to best suit the needs of the audio amplifier at each given instant.

There are a few patents that could help with this project. Patent US4218660A represents an audio amplifier and method that allows for a consistent match of the output signal to the audio amplifiers power requirements. "When the power requirements of the amplifier are either higher or lower, the duration of the current pulses to the transformer are made longer or shorter, respectively, to match the power requirements of the amplifier." Robert Carver's idea of matching the power requirements using a modulated signal is a very good approach to solving the power consumption issues associated with amplification; however, it is very hardware heavy and could possibly be very cost-ineffective [7].

Another patent that provides some helpful incite is Patent US11177092 which describes a class AB-D audio power amplifier that switches from one mode to another depending on the input frequency required to deliver the best quality output. The trade-off here is the fact that when switching between modes, there is an "overlapping" moment in time during the switching where some of the signal can be lost [8].

The proposed audio amplifier project can presumably be used almost anywhere where there is an audio amplifier. This technology can be implemented in cars, large concert speakers, store and restaurant audio systems, as well as personal audio devices. This results in a better listening experience for all while cutting down on power consumption. Cutting down on power consumption by being more power efficient saves money for large concert venues providing speakers, saves money for stores and restaurants providing music to their customers, and helps to

extend the battery life in vehicles and personal audio devices. Other systems such as PA systems in places such as schools, could also utilize this technology to help relay a clearer message.

      For this capstone project, an audio amplifier will be designed such that it will delay and read an input signal, subsequently, it will output a power-efficient amplified version of the input signal. The power of the output signal will be determined by a combination of the level of selected volume and input signal amplitude. To control the power of the output, the supply voltage will be varied to suit the needs of the signal, while minimizing the dissipated power. When the input voltage is small, the supply voltage need not be large, thus the supply voltage will be adjusted to a smaller level to minimize wasted power. Similarly, when the input voltage is large, the supply voltage will be reflective of this and will provide a larger value to ensure linearity. Upon implementation of this amplifier, a larger power efficiency can be achieved without sacrificing in audio output quality. This technology can may be implemented in vehicles, concert speakers, stores, restaurants, as well as personal music listening devices. The research for this project has been set forth to address important preliminary questions. There are many resources surrounding amplifiers that will help in designing the presented audio amplifier. This project has been shown to be feasible and to have potential for everyday application.

Marketing Requirements (AC)

1. The device should produce high quality audio for personal use.
2. The device should be power efficient.
3. The device should be capable of delivering at least twice the power that a conventional personal speaker is rated at.

4. The audio signal delay of the device should be minimal enough such that output is as close to real-time input as possible.

5. The device should have simple on/off capabilities.

6. The device should be compatible with conventional audio equipment.

7. The device should be powered by a 120 V 60 Hz receptacle.

Objective Tree (Figure 1): (AC, EV)
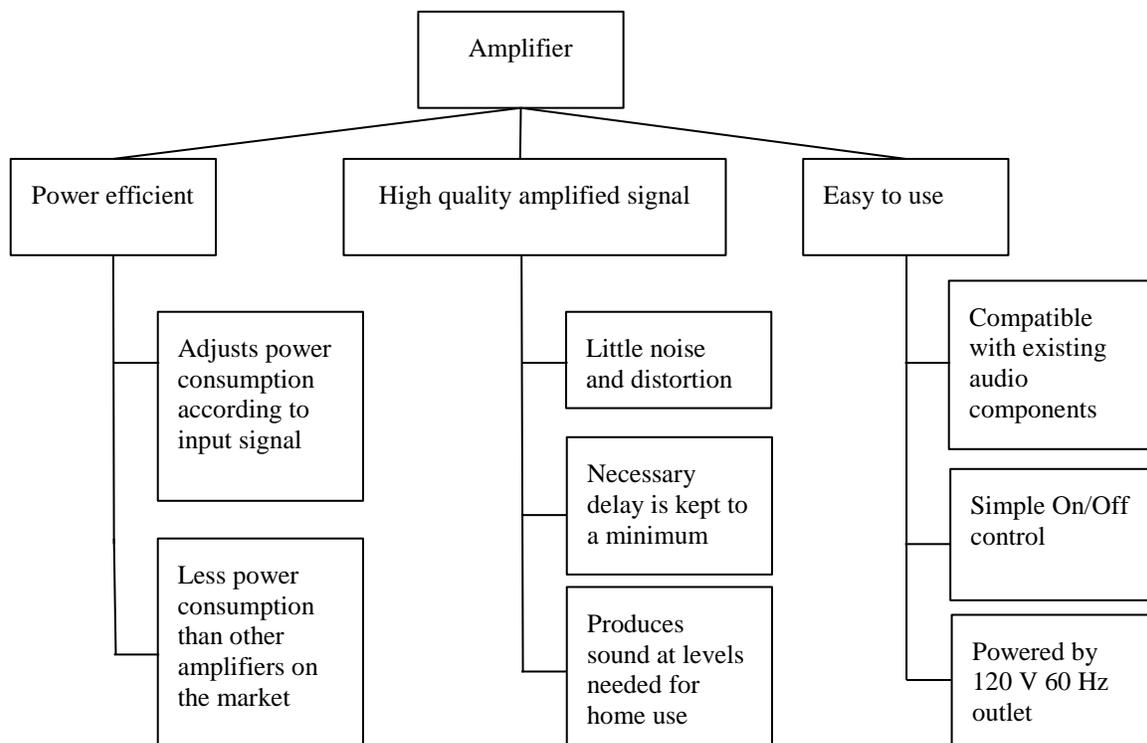
Figure 1

Figure 1 depicts an objective tree for the amplifier that is created in this project. It focuses on three aspects of the amplifier: power efficiency, high quality output signal, and ease of use. Each of the three aspects are then expanded upon within the proceeding branches.

Mechanical Sketch of System (Figure 2): (EV)
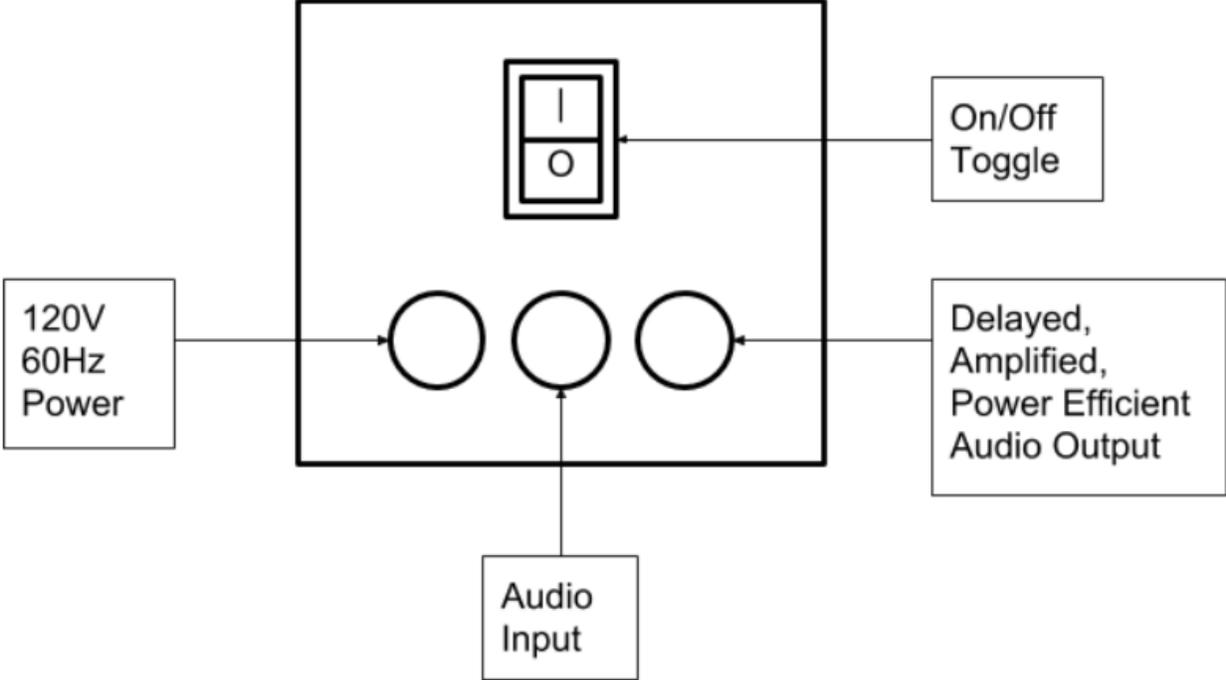
Figure 2

Figure 2 depicts a rough mechanical sketch of the audio amplifier. This includes the basic inputs and outputs of the amplifier. The inputs include the volume control, an on/off toggle switch, power input, and audio input. The output of the amplifier is an amplified audio output signal.

II. Design Requirements Specification (AC, TO, ST, EV)

Table 1

Marketing Requirments	Design Requirements	Justification
1	The device should have a signal to noise ratio of 40 dB or higher.	40 dB and higher is high SNR in audio.
2	The device should consume an average of 30% less power than a non-dynamic voltage rail amplifier.	Based on preliminary calculations, the speaker only needs about 66% of the power provided by a non-dynamic rail amplifier. An added 4% leaves room for power consumed by circuit components.
1, 2	The voltage rails should be changed quickly and accurately enough to avoid distortion.	Circuit component saturation can occur during slow rail switching leading to distortion and possible damage.
3, 6	The amplifier will have a gain of 20 dB.	Standard gain in audio amplifiers.
6	The device should allow input via 1/8" stereo cable.	1/8" stereo cables are widely used for audio signals.
7	The device should be powered by a 120 V, 60 Hz receptacle.	120 V, 60 Hz receptacles are standard in US.
2	6 V, 12 V, 18 V, and 24 V will be used as voltage rails for the power supply.	Based on calculations, 4 rails increase efficiency by 52% or more dependent on the signal.
4	The input will have at most a 10-millisecond delay.	The delay should be small enough so that there is no noticeable delay if the audio is synced with a video.
1	The amplifier should produce a frequency response between 20 Hz and 20 kHz.	This frequency response the range of sound observable by humans.
1	The amplifier will have a total harmonic distortion (THD) of 2% or less.	Sound quality deteriorates with higher THD percentages,

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III. Accepted Technical Design

Equations (EV)

1. $x = A * \sin(\omega t)$

2. $E = P * t = \left(\frac{V^2}{R}\right) * t$

3. $\text{Energy Decrease} = \left(\frac{E_{old} - E_{new}}{E_{old}}\right) * 100\%$

Variables:

1. $A = $ Amplitude (Volts)

2. $\omega = $ Radians (Radians)

3. $t = $ Time (Seconds)

4. $x = $ Signal Input Equation (Volts)

5. $P = $ Power Usage (Watts)

6. $V = $ Amplifier Voltage Equation

7. $R = $ Resistance (Ohms)

8. $E = $ Energy Used (Joules)

Engineering Calculations (AC, EV)

The main purpose of this project is to decrease wasted power in an audio amplifier circuit. In order to increase power efficiency, multiple voltage rails will be used, wherein the lowest required voltage rail will be applied as necessary to an amplifier. To demonstrate the benefit of this method, a sine wave with zero phase shift will be analyzed from 0 to pi seconds (positive portion of a sine wave) with amplitude $A = 16$ and frequency $\omega = 100$. These values may be used in equation 1 to describe the amplitude and frequency of x. In an embodiment, four

voltage rails are available: 4 V, 8 V, 12 V, and 16 V. Table 2 describes the times, and durations at which the sine wave reaches each of the rail voltage values.

Table 2

Required Rail Voltage [V]	Time Interval(s) [ms]	Total Time [ms]
4	0 - 2.53, 28.88 – 31.41	5.06
8	2.53 - 5.24, 26.17 – 28.88	5.42
12	5.24 - 8.48, 22.93 – 26.17	6.48
16	8.48 – 22.93	14.45
TOTAL	N/A	31.41

Given a standard speaker load of $R = 8\Omega$, equation 2 is used to determine the total energy consumed by the sine wave. The dynamic rails will expend a total of 0.63252 J. If we assume that a microcontroller draws 100 mW and each of the 4 rail switches dissipates 200 mW, then the Joules expended becomes 0.660789. In contrast, a non-dynamic (stationary) voltage rail which remains constant at 16 V would expend 1.00512 J for the same sine wave. Using equation 3, it is clear that switching between four rail voltage values, even with added circuitry, decreases energy consumption by over 34%.

Using MATLAB Student, a more detailed simulation for energy consumption using dynamic rail voltages was generated. Executing the code in Appendix A derives that the Dynamic Rail system requires an average of 14.2712W, whereas the Constant Rail system requires 50W. This simulation illustrates that the Dynamic Rail System uses 71.4576% less power for the given conditions. In systems with a constant rail, much of the provided voltage is wasted. The above code was modified to simulate the percent decrease in power consumption for

multiple music types and different rail configurations. The results of these simulations are given

in Table 3 below:

Table 3

Music Genre	Rail Levels	% Decrease in Power
Classical	5,10,15,20	71.46
Jazz	5,10,15,20	16.79
Dance	5,10,15,20	18.57
Rock	5,10,15,20	60.14
Punk	5,10,15,20	6.86
Classical	2,4,8,16	64.53
Jazz	2,4,8,16	8.60
Dance	2,4,8,16	7.34
Rock	2,4,8,16	48.62
Punk	2,4,8,16	4.12
Classical	2,10,14,16	58.77
Jazz	2,10,14,16	18.55
Dance	2,10,14,16	29.12
Rock	2,10,14,16	55.28
Punk	2,10,14,16	9.67

The above calculations assume there are 4 Mosfet switches that consume 300mW

each, and the load is 8Ω. It can be calculated that the best rail configuration is the evenly

spaced configuration (5, 10, 15, and 20V) and the average % Decrease in power for this

configuration is 34.764%.

The code in Appendix A was modified once again to calculate % Decrease in power for

situations with more than 4 possible rails. Using classical music and evenly spaced rails, 4 rails

resulted in a 71.46% decrease in power, 5 rails resulted in a 73.20% decrease in power, and 6

rails resulted in a 73.77% decrease in power. Although there is a slight increase in efficiency for

more than 4 rails, the increase is insignificant when compared to the added complexity to the

design. Therefore, 4 evenly spaced rails will be used in the design.

Whether or not a delay of the audio signal is required must be determined. Assume that an Analog to Digital converter takes 16ns to generate a sample, and the MOSFET switch for each rail takes 21ns. If the sample rate is 48 kHz, then there is a total of 20,833 ns between samples. This value minus the delays of the Analog to Digital converter and MOSFET switches leaves 20,796 ns for code to run. Assuming a microcontroller operating at 70 MHz, this gives 1,455 clock cycles for code to be executed.

A measure of how quickly the signal can change should be determined. Assume the highest frequency audio signal is 20 kHz or 125,663.7061 r/s. Assume the maximum amplitude of the signal is 1.75 V. This yields the following equation:

$$x(t) = 24 \sin(125663.7061 \times t)$$

If the lowest rail is used when the signal is of maximum amplitude 0.4375 V and the next highest rail is at 0.875 V, the values of 0.4375 V and 0.875 V can be inserted for x and solving for t will yield the time it takes for the signal to travel to each value. Taking the difference of the results of t will yield the minimum time it takes for the signal to travel from one rail value to the next. Upon calculation, the signal can travel from one rail to the next in only 2.155 μs. That is, the signal can change by 0.4375V every 2.155 μs. Assume a MOSFET switch with a delay of 50 ns is used to control the rails. Using the above calculation, the signal can only change by 204 μV during the MOSFET delay. Therefore, it can be concluded that if the rail is switched higher any time the signal is within 204 μV of the next higher rail, any chance of clipping the signal can be eliminated.

Level 0 Block Diagram (Figure 3): (AC, EV)
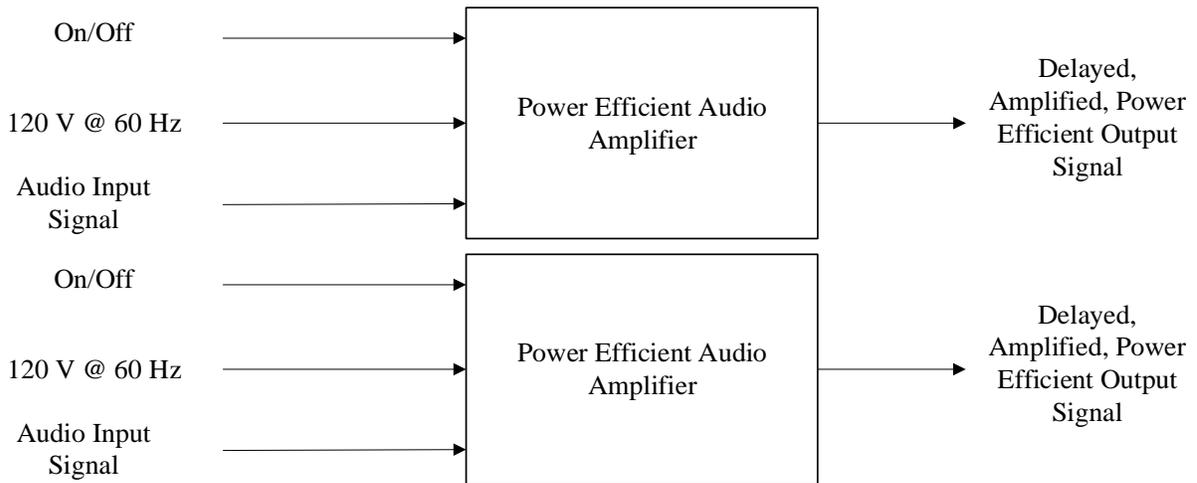
Figure 3

      Figure 3 depicts a Level 0 block diagram of the amplifier created in this project. It shows

the three desired inputs for the amplifier on the left side, and the desired output on the right.

Level 0 Functional Requirement Table: (AC, TO, ST, EV)

Table 4

Module	Power Efficient Power Amplifier
Designer	DT01
Inputs	- Audio Input Signal: ~0.5 V - 120 V @ 60 Hz power - On/Off
Outputs	- Delayed, Amplified, Power efficient audio output signal
Functionality	- Read the Audio Input Signal and determine the necessary power usage.

Level 1 Block Diagram (Figure 4): (TO, EV)
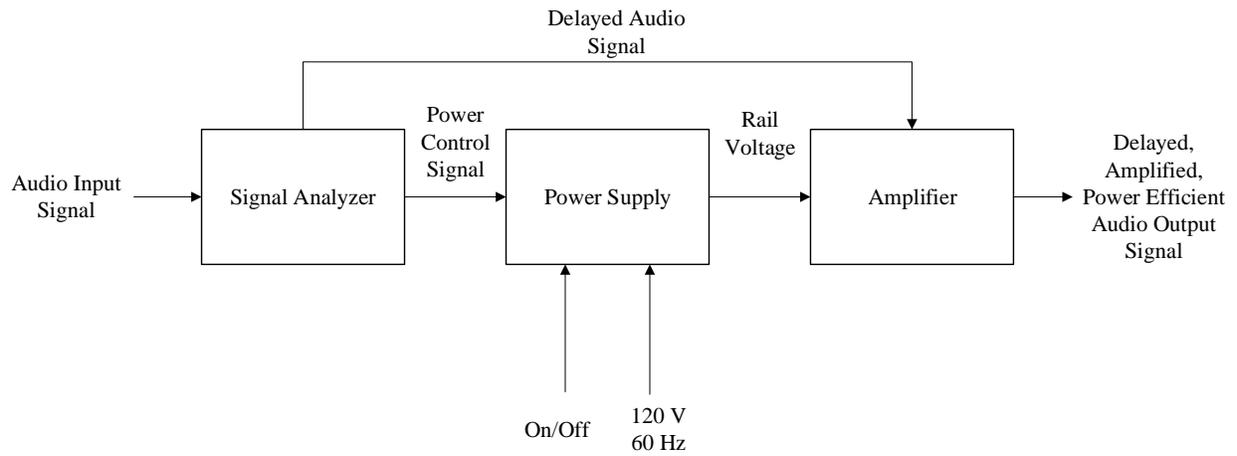
Figure 4

Figure 4 illustrates a level-1 block diagram of the same amplifier shown in Figure 3.

Figure 4 describes in more detail the various stages of the amplifier. The total input and output of

the amplifier remain the same as in the Level 0 Block Diagram.

Level 1 Functional Requirement Tables: (AC, TO, ST, EV)

Table 5

Module	Signal Analyzer
Designer	**Andrew Cantrell, Evan Von Duhn**
Inputs	- **Audio Input Signal: ~0.5 V**
Outputs	- **Power Control Signal: 0.5 V** - **Delayed Audio Input Signal: ~0.5 V**
Functionality	- **Read the Audio Input Signal and determine the necessary power usage.**

Table 6

Module	Power Supply
Designer	**Timothy Oshatyuk, Slavisa Tosanovic**
Inputs	- **Power Control Signal** - **On/Off** - **Power: 120 V 60 Hz**
Outputs	- **Rail Voltages: Dynamic $\pm$(0-20 V)**
Functionality	- **Adjust the rail voltages according to the required power.**

Table 7

Module	Amplifier
Designer	**Timothy Oshatyuk, Slavisa Tosanovic**
Inputs	- **Audio Input Signal: ~0.5 V** - **Rail Voltages: Dynamic, changes based on the input signal.**
Outputs	- **Delayed, Amplified, Power Efficient Output Audio Signal: $\pm$(0 - 50 V)**

Functionality	- Amplify the Audio Input Signal to match 400W, 8 Ω

Table 8

Module	Software
Designer	Andrew Cantrell
Inputs	- Audio Input Signal
Outputs	- Power Control Signal
Functionality	- Sample the input audio at a rate of 44.1 kHz and find required power for amplified signal, sending that data to the power supply.

Level 2 Signal Analyzer Block Diagram (Figure 5): (AC, EV)
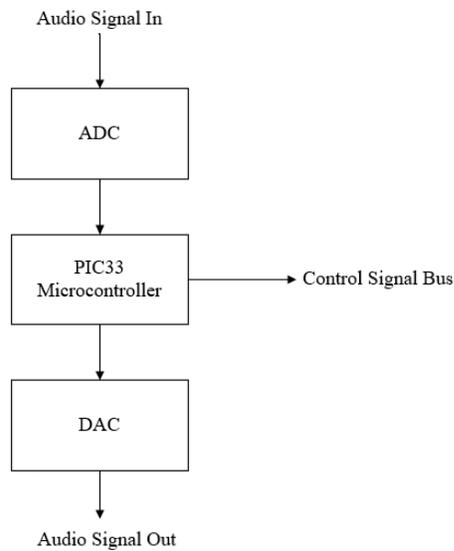
Figure 5

Figure 5 depicts the level-2 block diagram for the signal analyzer. The purpose of the

signal analyzer is to generate a group of control signals which will be used to activate the necessary rail

for the incoming audio signal and deactivate the other unnecessary rails. To accomplish this, the audio

signal will be sampled by an analog to digital converter. The resulting discrete values will be analyzed in software on a PIC33 microcontroller to determine which rail must be active. Based on the software results, a bus from the I/O pins of the PIC33 will turn on the required rail and turn the other rails off. The discrete values of the audio signal will then be sent to a digital to analog converter to be converted back to the original analog audio signal, which will be used by the amplifier.

Level 2 Signal Analyzer Functional Requirement Tables: (AC)

Table 9

Module	ADC
Designer	n/a- purchased
Inputs	Analog Audio Signal 3.5 V peak to peak
Outputs	Quantized, discrete values from Analog Audio Signal
Functionality	The ADC will convert the incoming analog signal into discrete values to be read by the microcontroller. This should be done at a sample rate of 44.1 kHz of higher.

Table 10

Module	PIC33 Microcontroller
Designer	Programmed by Andrew Cantrell, Evan Von Duhn
Inputs	Discrete Quantized Audio Samples
Outputs	Power Control Signals, Audio Samples
Functionality	The PIC Microcontroller will run the code needed to determine which rail is needed for the audio signal and will generate a control signal to be used by the power supply to turn on the needed rail and turn unnecessary rails off. This will be realized with a control bus, each wire of the bus controlling a different rail.

Table 11

Module	DAC
Designer	**Programmed by Andrew Cantrell, Evan Von Duhn**
Inputs	**Discrete Quantized Audio Samples**
Outputs	**Analog Audio Signal**
Functionality	**The DAC is included in the PIC Microcontroller and will convert the digital audio back into analog audio which will be amplified by the amplifier circuit.**

Level 2 Power Supply Block Diagram (Figure 6): (TO, ST)
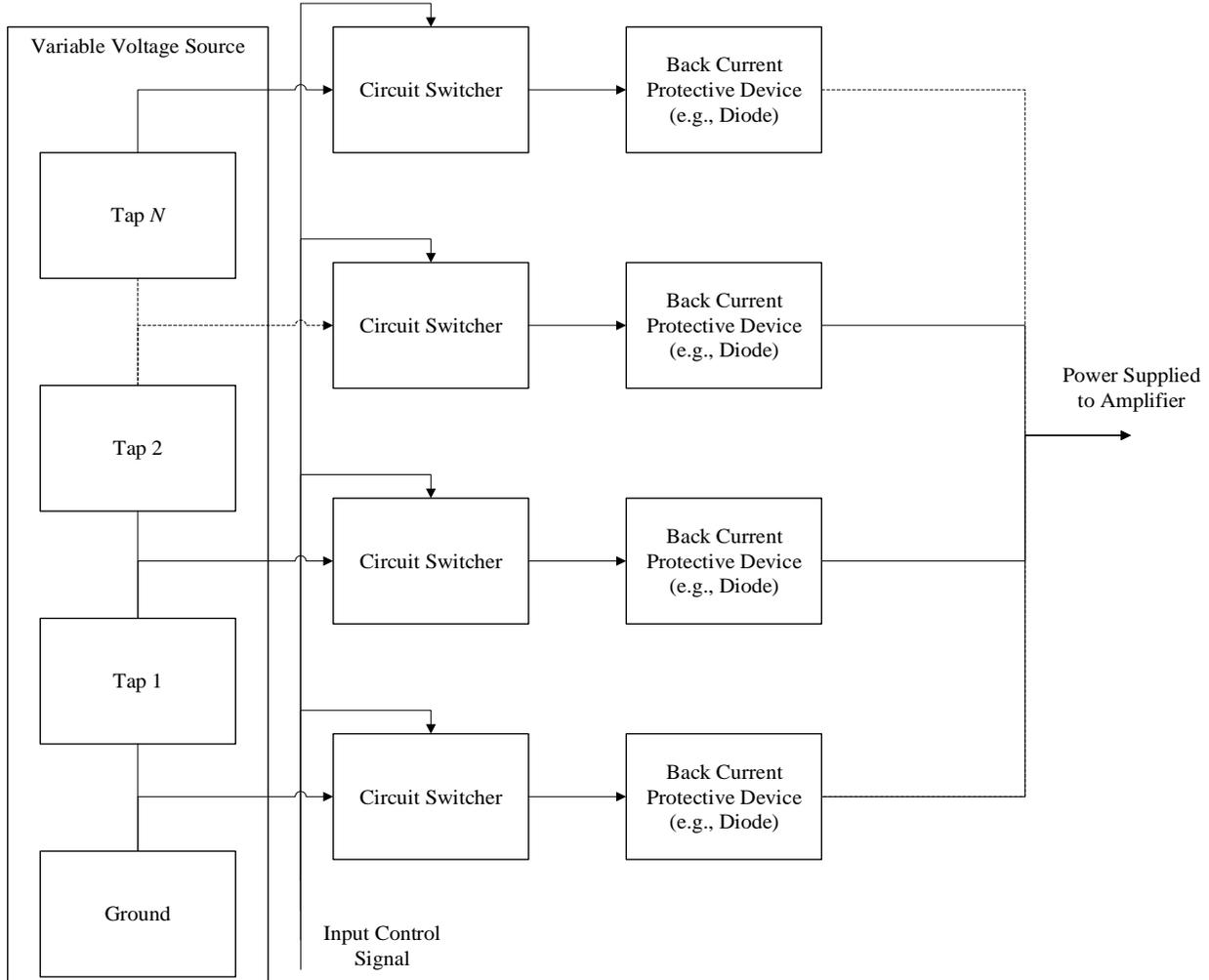
Figure 6

Figure 6 depicts a level 2 block diagram for the power supply of figure 4. A series of

batteries whose voltages can be added together to form discrete voltage levels are shown on the

left. Each level can be achieved by having the input control signal activate one switch at a time

allowing for current flow through a set amount of batteries whose voltage will be used to power

the amplifier. A unilateral element, such as a diode, is placed in series after each relay to protect

the batteries from back current which can cause damage.

Table 12

Module	Tap
Designer	n/a - purchased
Inputs	- **Current from active circuit switcher**
Outputs	- **Varied DC voltage depending on transformer tap value**
Functionality	- **Provide voltage to the amplifier depending on the tap active in the string at a given point of time.**

Table 13

Module	Circuit Switcher
Designer	n/a - purchased
Inputs	- **Input control signal from the microcontroller**
Outputs	- **"Switch on command" (internal)**
Functionality	- **Opens or closes based on the incoming control signal. Depending on which relay is open determines the amount of voltage provided by the power supply.**

Table 14

Module	Back Current Protective Device
Designer	n/a - purchased
Inputs	- **Current Flow from transformer to amplifier**
Outputs	- **Current Flow from transformer to amplifier**
Functionality	- **Prevents reverse current from flowing back into the transformer.**

Level 2 Amplifier Block Diagram (Figure 7): (TO, ST)
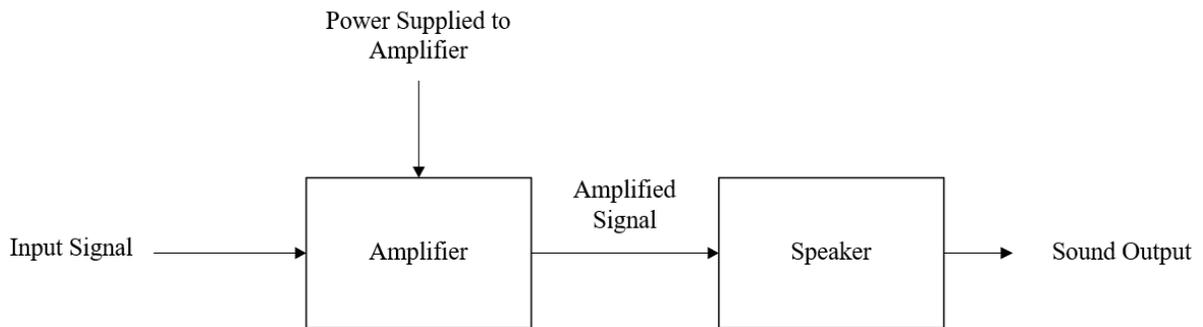
Figure 7

Table 15

Module	Amplifier
Designer	Timothy Oshatyuk, Slavisa Tosanovic
Inputs	- **Delayed audio input signal**
Outputs	- **Amplified audio signal**
Functionality	- **Amplifies a small electrical audio signal to be played on a speaker**

Table 16

Module	Speaker
Designer	n/a - purchased
Inputs	- **Amplified audio signal**
Outputs	- **Power/Sound**
Functionality	- **A speaker that matches appropriate values to operate with the amplifier, which allows the user to listen to their music.**

High Level Software Flow Chart (Figure 8): (AC, EV)
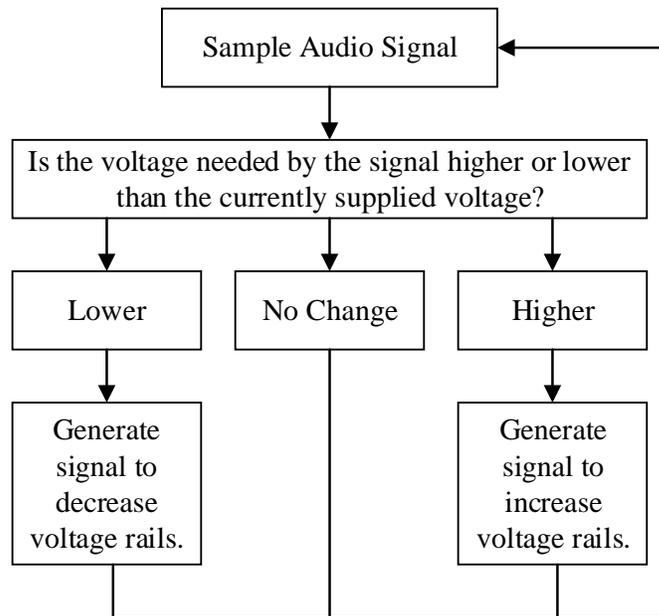
Figure 8

Figure 8 describes how the software running in the embedded controller will sample the audio signal input and determine how the voltage rails for the amplifier should change. If there is a needed change in the voltage rails, then the embedded controller will send a signal to the power supply indicating how to change the rail voltages. Note that the sampling rate will be 48

kHz and the dsPIC33 can complete 40 M instructions per second. Therefore, the code can complete only 833 instructions per sample, so the simpler the code, the better.

Pseudocode (AC)

-Set global constants for the different rail levels. These constants will be compared to the signal to see which threshold the signal is within. (Using the information gained in the engineering calculations section, the rail should be changed higher anytime the signal is within 204 μV of the next highest rail for an incoming 1.75 V amplitude signal. For rails at 6, 12, 18, and 24 V, if the incoming signal has an amplitude of 0 V – 0.437296 V, the 6V rail is needed. For an input between 0. 437296 V - 0.874796 V, the 12 V rail is needed. For an input between 0.874796 V – 1.312296 V, the 18 V rail is needed. Finally, for an input greater than 1.312296 V, the 24 V rail is required.)

-Set a Timer Interrupt to occur with a frequency equal to the desired sample frequency (e.g. 48kHz)

-During each interrupt service routine:

    -Retrieve samples for both left and right audio from the ADC.

    -If the samples lie in the highest threshold, set the rail to the highest rail.

    -Else, if the samples lie in the next lower threshold, set the rail to the next lower rail.

    -Else, if the samples lie in the next lower threshold, set the rail to the next lower rail.

    -Else, set the rail to the lowest rail.

    -Send the samples to the DAC for conversion back to analog audio.

    -Clear the interrupt flag.

Schematics (AC, TO, ST, EV)

Amplifier Schematic (Figure 9): (ST, EV)

Amplifier Schematic Theory (ST)

A class D amplifier IC was selected due to class D amplifiers being the most power efficient variation of amplifier while simultaneously not reducing sound quality to a noticeable degree. The TPA3031D2 amplifier has a maximum possible SNR value of 102dB as well as having a THD value of under 1% in most conditions, however the THD can reach 10% at max power output, but on average that is not common, and the average THD value would still be under 1%. The amplifier will receive 4 incoming signals from the micro controller. These 4 signals are the positive audio input for the left and right speaker as well as negative for the left and right speaker. The amplifier will be receiving its changing rail voltages from the power supply. Decoupling capacitors were added in parallel to protect the amplifier IC from any high frequency noise that could be present in our power supply. The TPA3130D2 specification sheet provides many resistor relations to obtain different gain values, in order to obtain a gain of 20 dB, a 100 kΩ resistor and a 20 kΩ resistor were used for R1 and R2 respectively. An LC low pass filter is used on the output stage of the amplifier before the speakers. The low pass filter is used to filter out the high frequency component created by the pulse width modulation of class D amplifiers. Lastly, speakers were selected to match the output power of the amplifier in stereo mode which was 25W.

Microcontroller Schematic (Figure 10): (AC, ST, EV)
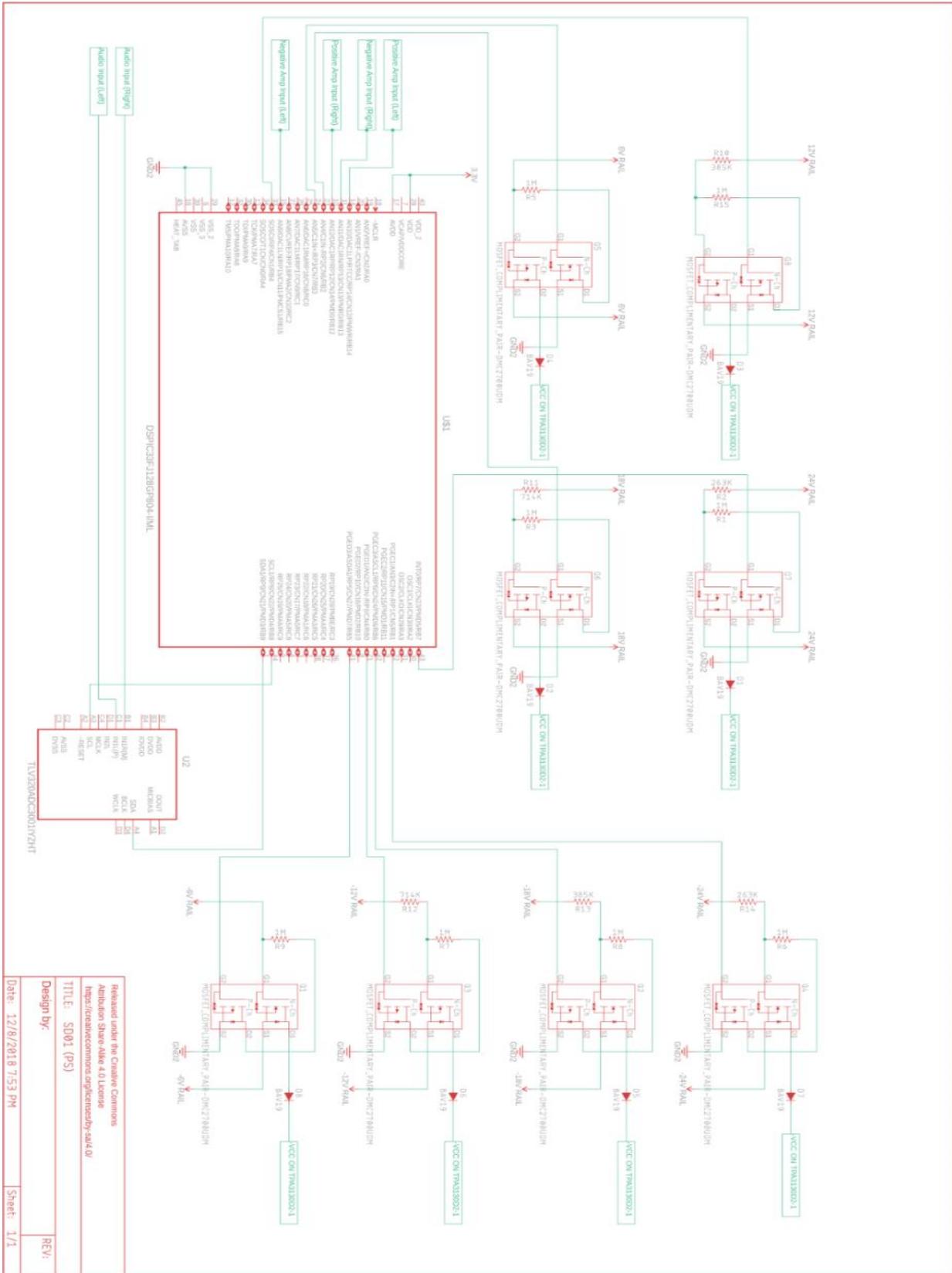
Microcontroller Schematic Theory (AC)

The microcontroller circuit is responsible for allowing a particular set of rails to power

the amplifier circuit based on the power requirements of an incoming audio signal. The audio

signal is first received by the TLV320ADC3001 which converts the analog audio signal into digital

samples. The TLV320ADC3001 was chosen in part due to its Signal-to-Noise ratio of 92 dB, well above

the design requirement of 40 dB. The dsPIC33FJ128GP804 communicates with the

TLV320ADC3001 using I2C serial communication in order to receive the audio samples. The dsPIC33

will then run code to determine the rail voltage required by the audio signal. Based on the software

results, the dsPIC33 will set the values of 8 of its I/O pins. Each of these 8 I/O pins are connected to a

FDG6322C IC which includes both an NMOS and a PMOS. These MOSFETS are configured in such a

way that an incoming signal will allow them to pass a certain voltage that they are connected to. For the

positive rails, this is done by connecting the drain of the NMOS to the gate of the PMOS through a

resistor. When the NMOS is on, it will allow current flow through the two resistors connected to the

FDG6322C. The two resistors create a voltage divider that set the gate voltage of the PMOS to an

appropriate level to reach saturation, allowing the PMOS to pass the rail voltage from its source to drain.

For the negative rails, the drain of the PMOS is connected to the gate of the NMOS through a resistor.

When the PMOS is on, it will allow current flow through the two resistors connected to the FDG6322C.

The two resistors create a voltage divider that set the gate voltage of the NMOS to an appropriate level to

reach saturation, allowing the NMOS to pass the rail voltage from its source to drain. The dsPIC33

supplies the incoming signal to each FDG6322C and depending on the dsPIC33 signal, the FDG6322C

will either pass or block the rail that it is connected to. After the appropriate rail has been set, the

dsPIC33FJ128GP804 will use an internal DAC to convert the audio back into analog with a

signal-to-noise ratio of 90 dB.

Power Supply Schematic (Figure 11): (TO, ST)

TITLE: SD81 Power Supply

Design by:

Date: 12/8/2018 8:01 PM

Sheet: 1/1

REV:

Power Supply Schematic Theory (TO, ST)

The power supply is responsible for providing eight discrete different voltage rails which are ±6 V, ±12 V, ±18 V, and ±24 V. As shown in the schematic, 120 VAC (standard wall receptacle voltage) will be supplying power to a 4 multitap transformers with 6 V, 12 V, and 18 V on the secondary side. In order to obtain the 24 V rail, the 6 V and 18 V secondary windings will be connected. The AC voltage from the transformer will be rectified to DC using a full wave bridge rectifier IC. The orientation of the rectifiers will determine which rails are positive and which are negative by which pin is used as the output and which will be grounded. Lastly a 1000uF capacitor follows each rectifier to hold a steady DC voltage to be used for the amplifier rails. Each rail is determined to be in use by the FDG6322C transistors in the microcontroller schematic.

Theory of Operation (AC)

The objective of this project is to create an audio amplifier that uses dynamic voltage rails in order to decrease power consumption. The design will have multiple rails that can be applied based on the needs of the signal. The multiple voltages will be supplied by stringing multiple batteries in series and having leads from different points in the string. For example, three 1.5 V batteries in series can give incremental voltages of 0 V (no battery connected), 1.5 V (one battery), 3.0 V (two batteries), and 4.5 V (all three batteries). A challenge is to be able to switch between the rails without supplying power to the switches. Only one switch will be activated at a time, allowing for one voltage rail to operate at a time. An analysis of possible switches is given in Table 19.

Table 17

Switch	Delay	Power Dissipation
KT00-1A-40L-XXX Reed Relay	1.1ms	138-320mW
PLA172P Solid State Relay	.5ms	550mW
EC2-5TNU Latch Relay	2ms	140mW
FDG6321C Dual N & P Channel Digital FET	21ns	300mW

In order to choose the rails, envelope analysis of the audio signal must be available. The rail may be selected based on the amplitude of the audio signal. The software will sample the incoming audio signal and take the absolute value. This value will then be compared to the previous sample stored in some variable called Sample. If the new sample is higher than Sample, then Sample will be set to the new sample. However, if the new sample is smaller than Sample, then Sample will be decremented by some fixed amount. The value stored in Sample can then be compared against threshold values to determine appropriate the voltage rail. The incoming audio signal (after rectification) will be between 0 V and 1.75 V. It is assumed that the possible voltage rail values are ±6 V, ±12 V, ±18 V, and ±24 V and that there is a linear relationship between the incoming signal and the rail voltage required. If the incoming signal has an amplitude of 0 V – 0.4375 V, the 6 V rail is needed. For an input between 0.4375 V - 0.875 V, the 12 V rail is needed. For an input between 0.875 V – 1.3125 V, the 18 V rail is needed. Finally, for an input greater than 1.3125 V, the 24 V rail is required.

IV. Parts List (TO, AC)

Table 18

Qty.	Refdes	Part Num.	Description
10	Q1-Q8 (AMP/MC)	FDG6322C	MOSFET SC70-6 COMP N-P-CH
10	N/A	33006	PROTO BOARD ADAPTER SMT SOT-363
2	N/A	PA0063	QFN-20 TO DIP-20 SMT ADAPTER
4	TR1-TR8 (PS)	596	Class 2 Transformer, Input Voltage: 120VAC, Output Voltage: 6.0VAC, 12VAC, 18VAC
1	U2 (MC)	DM240001-3	Explorer 16/32 Development Kit
3	N/A (AMP)	TPA3130D2DAPR	Class D Amplifier
1	U1 (MC)	MA330019	dsPIC33FJ128GP804 44P QFN to 100P Plug-In Module
8	D1-D8 (PS)	MB4S-TP	BRIDGE RECT 1P 400V 500MA MBS-1
10	C1-C7,C9,C10 (AMP)	C320C105K5N5TA91707301	1 uF capacitor
6	C8,C11-C15 (AMP)	EEU-FS1K221	220 uF capacitor
1	R1 (AMP)	EEU-FS1H102L	100 kΩ resistor
1	R2 (AMP)	HHV-25JT-52-20K	20 kΩ resistor
4	L1-L4 (AMP)	RLB0914-100KL	10 uH inductors
2	SP1, SP2 (AMP)	AS06008PS-R	SPEAKER 8OHM 10W TOP PORT 99DB
8	C1-C8 (PS)	EEU-FS1H102L	1 mF capacitor
8	D1-D8 (MC)	BAV19-TR	Diodes for microcontroller
4	C16-C19 (AMP)	FG28X7R1E684KRT06	660 nF capacitors
8	R1,R3,R5-R9,R15 (MC)	CMF601M0000BEEK	1 MΩ resistor
2	R2,R14 (MC)	MF0207FTE52-270K	263 kΩ resistor
2	R11,R12 (MC)	MF1/4DCT52R7153F	714 kΩ resistor
2	R10,R13 (MC)	MBA02040C3833FRP00	385 kΩ resistor

Table 19

Qty.	Part Num.	Description	Unit Cost	Total Cost
10	FDG6322C	MOSFET SC70-6 COMP N-P-CH	$0.33	$3.32
10	33006	PROTO BOARD ADAPTER SMT SOT-363	$2.20	$22.00
2	PA0063	QFN-20 TO DIP-20 SMT ADAPTER	$5.29	$10.58
4	596	Class 2 Transformer, Input Voltage: 120VAC, Output Voltage: 6.0VAC, 12VAC, 18VAC	$22.20	$88.80
1	DM240001-3	Explorer 16/32 Development Kit	$109.99	$109.99
3	TPA3130D2DAPR	Class D Amplifier	$2.81	$8.43
1	MA330019	dsPIC33FJ128GP804 44P QFN to 100P Plug-In Module	$25.00	$25.00
8	MB4S-TP	BRIDGE RECT 1P 400V 500MA MBS-1	$0.40	$3.20
10	C320C105K5N5TA91707301	1 uF capacitor	$0.55	$5.47
6	EEU-FS1K221	220 uF capacitor	$0.95	$5.70
1	HHV-50FR-52-100K	100 kΩ resistor	$0.48	$0.48
1	HHV-25JT-52-20K	20 kΩ resistor	$0.34	$0.34
4	RLB0914-100KL	10 uH inductors	$0.40	$1.60
2	AS06008PS-R	SPEAKER 8OHM 10W TOP PORT 99DB	$21.67	$43.34
8	EEU-FS1H102L	1 mF capacitor	$1.66	$13.28
8	BAV19-TR	Diodes for microcontroller	$0.17	$1.36
4	FG28X7R1E684KRT06	660 nF capacitors	$0.30	$1.20
8	CMF601M0000BEEK	1 MΩ resistor	$1.33	$10.64
2	MF0207FTE52-270K	263 kΩ resistor	$0.12	$0.24
2	MF1/4DCT52R7153F	714 kΩ resistor	$0.23	$0.46
2	MBA02040C3833FRP00	385 kΩ resistor	$0.14	$0.28
			TOTAL	$355.71

V. Project Schedules (TO, EV)

Task Name	Duration	Start	Finish	Resource Names
SDP1 Fall 2018				
Project Design				
Preliminary report	11 days	Thu 9/6/18	Sun 9/16/18	Andrew Cantrell,Timothy Oshatyuk,Slavisa Tosanovic,Evan Von Duhn
Cover page	11 days	Thu 9/6/18	Sun 9/16/18	
T of C, L of T, L of F	11 days	Thu 9/6/18	Sun 9/16/18	
Need	11 days	Thu 9/6/18	Sun 9/16/18	
Objective	11 days	Thu 9/6/18	Sun 9/16/18	
Background	11 days	Thu 9/6/18	Sun 9/16/18	
Marketing Requirements	11 days	Thu 9/6/18	Sun 9/16/18	
Objective Tree	11 days	Thu 9/6/18	Sun 9/16/18	
Block Diagrams Level 0, 1, ... w/ FR tables	**11 days**	Thu 9/6/18	Sun 9/16/18	
Hardware modules (Timothy Oshatyuk, Slavisa Tosanovic)	**11 days**	**Thu 9/6/18**	**Sun 9/16/18**	
Power Supply	11 days	Thu 9/6/18	Sun 9/16/18	Timothy Oshatyuk
Amplifier	11 days	Thu 9/6/18	Sun 9/16/18	Slavisa Tosanovic
Software modules (Andrew Cantrell, Evan Von Duhn)	**11 days**	**Thu 9/6/18**	**Sun 9/16/18**	
Signal Analyzer				Andrew Cantrell,Evan Von Duhn
Team information	11 days	Thu 9/6/18	Sun 9/16/18	
References	11 days	Thu 9/6/18	Sun 9/16/18	
Preliminary Parts Request Form	11 days	Thu 9/6/18	Sun 9/16/18	
Midterm Report	**35 days**	**Thu 9/6/18**	**Wed 10/10/18**	Andrew Cantrell,Timothy Oshatyuk,Slavisa Tosanovic,Evan Von Duhn

Design Requirements Specification	14 days	Mon 9/17/18	Sun 9/30/18	
Midterm Design Gantt Chart	24 days	Mon 9/17/18	Wed 10/10/18	Timothy Oshatyuk
Design Calculations	**24 days**	**Mon 9/17/18**	**Wed 10/10/18**	
Electrical Calculations	**24 days**	**Mon 9/17/18**	**Wed 10/10/18**	
Communication	24 days	Mon 9/17/18	Wed 10/10/18	Andrew Cantrell,Evan Von Duhn
Computing	24 days	Mon 9/17/18	Wed 10/10/18	Andrew Cantrell,Evan Von Duhn
Control Systems	24 days	Mon 9/17/18	Wed 10/10/18	Andrew Cantrell,Evan Von Duhn
Power, Voltage, Current	24 days	Mon 9/17/18	Wed 10/10/18	Timothy Oshatyuk,Slavisa Tosanovic
Block Diagrams Level 2 w/ FR tables & ToO	**24 days**	**Mon 9/17/18**	**Wed 10/10/18**	
Hardware modules (Timothy Oshatyuk, Slavisa Tosanovic)	24 days	Mon 9/17/18	Wed 10/10/18	Timothy Oshatyuk,Slavisa Tosanovic
Software modules (Andrew Cantrell, Evan Von Duhn)	24 days	Mon 9/17/18	Wed 10/10/18	Andrew Cantrell,Evan Von Duhn
Block Diagrams Level 3 w/ FR tables & ToO	**17 days**	**Mon 9/24/18**	**Wed 10/10/18**	
Hardware modules (Timothy Oshatyuk, Slavisa Tosanovic)	17 days	Mon 9/24/18	Wed 10/10/18	Timothy Oshatyuk,Slavisa Tosanovic
Software modules (Andrew Cantrell, Evan Von Duhn)	17 days	Mon 9/24/18	Wed 10/10/18	Andrew Cantrell,Evan Von Duhn
Midterm Design Presentations Part 1	1 day	Thu 10/11/18	Thu 10/11/18	Andrew Cantrell,Timothy Oshatyuk,Slavisa Tosanovic,Evan Von Duhn
Midterm Design Presentations Part 2	1 day	Thu 10/18/18	Thu 10/18/18	
Project Poster	14 days	Mon 10/8/18	Sun 10/21/18	Andrew Cantrell,Timothy Oshatyuk,Slavisa Tosanovic,Evan Von Duhn
Secondary Parts Request Form	21 days	Mon 9/17/18	Sun 10/7/18	
Final Design Report	**52 days**	**Mon 10/8/18**	**Wed 11/28/18**	Andrew Cantrell,Timothy Oshatyuk,Slavisa

Task Name	Duration	Start	Finish	Predecessors	Resource Names
					Tosanovic,Evan Von Duhn
Abstract	52 days	Mon 10/8/18	Wed 11/28/18		Evan Von Duhn
Software Design	**31 days**	**Mon 10/8/18**	**Wed 11/7/18**		
Modules 1…n	**31 days**	**Mon 10/8/18**	**Wed 11/7/18**		
Psuedo Code	31 days	Mon 10/8/18	Wed 11/7/18		Andrew Cantrell,Evan Von Duhn
Hardware Design	**31 days**	**Mon 10/8/18**	**Wed 11/7/18**		
Modules 1…n	**31 days**	**Mon 10/8/18**	**Wed 11/7/18**		
Simulations	31 days	Mon 10/8/18	Wed 11/7/18		Andrew Cantrell,Evan Von Duhn
Schematics	31 days	Mon 10/8/18	Wed 11/7/18		Timothy Oshatyuk,Slavisa Tosanovic
Parts Lists	**52 days**	**Mon 10/8/18**	**Wed 11/28/18**		
Parts list(s) for Schematics	52 days	Mon 10/8/18	Wed 11/28/18		Timothy Oshatyuk,Slavisa Tosanovic
Materials Budget list	52 days	Mon 10/8/18	Wed 11/28/18		Timothy Oshatyuk,Slavisa Tosanovic
Proposed Implementation Gantt Chart	52 days	Mon 10/8/18	Wed 11/28/18		Andrew Cantrell,Timothy Oshatyuk,Slavisa Tosanovic,Evan Von Duhn
Conclusions and Recommendations	52 days	Mon 10/8/18	Wed 11/28/18		Andrew Cantrell,Evan Von Duhn
Final Design Presentations Part 1	1 day	Thu 11/8/18	Thu 11/8/18		Andrew Cantrell,Timothy Oshatyuk,Slavisa Tosanovic,Evan Von Duhn
Final Design Presentations Part 2	1 day	Thu 11/15/18	Thu 11/15/18		
Secondary Parts Request Form	14 days	Thu 10/4/18	Wed 10/17/18		Timothy Oshatyuk,Slavisa Tosanovic
Final Parts Request Form	56 days	Mon 10/8/18	Sun 12/2/18		Timothy Oshatyuk,Slavisa Tosanovic

Task Name	Duration	Start	Finish	Predecessors	Resource Names
SDPII Implementation 2019	**103 days**	**Mon 1/14/19**	**Fri 4/26/19**		
Revise Gantt Chart	14 days	**Mon 1/14/19**	Sun 1/27/19		Andrew Cantrell,Timothy Oshatyuk,Slavisa Tosanovic,Evan Von Duhn

38

Implement Project Design	96 days	Mon 1/14/19	Fri 4/19/19		
Hardware Implementation	56 days	Mon 1/14/19	Sun 3/10/19		
Breadboard Components	13 days	Mon 1/14/19	Sat 1/26/19		Timothy Oshatyuk,Slavisa Tosanovic
Layout and Generate PCB(s)	14 days	Sun 1/27/19	Sat 2/9/19	5	Timothy Oshatyuk,Slavisa Tosanovic
Assemble Hardware	7 days	Sun 2/10/19	Sat 2/16/19	6	Timothy Oshatyuk,Slavisa Tosanovic
Test Hardware	14 days	Sun 2/17/19	Sat 3/2/19	7	Timothy Oshatyuk,Slavisa Tosanovic
Revise Hardware	14 days	Sun 2/17/19	Sat 3/2/19	7	Timothy Oshatyuk,Slavisa Tosanovic
MIDTERM: Demonstrate Hardware	5 days	Sun 3/3/19	Thu 3/7/19	8	Timothy Oshatyuk,Slavisa Tosanovic
SDC & FA Hardware Approval	0 days	Fri 3/8/19	Fri 3/8/19	10	Timothy Oshatyuk,Slavisa Tosanovic
Software Implementation	56 days	Mon 1/14/19	Sun 3/10/19	11	
Develop Software	27 days	Mon 1/14/19	Sat 2/9/19		Andrew Cantrell,Evan Von Duhn
Test Software	21 days	Sun 2/10/19	Sat 3/2/19	13	Andrew Cantrell,Evan Von Duhn
Revise Software	21 days	Sun 2/10/19	Sat 3/2/19	13	Andrew Cantrell,Evan Von Duhn
MIDTERM: Demonstrate Software	5 days	Sun 3/3/19	Thu 3/7/19	15	Andrew Cantrell,Evan Von Duhn
SDC & FA Software Approval	0 days	Fri 3/8/19	Fri 3/8/19	16	Andrew Cantrell,Evan Von Duhn
System Integration	42 days	Sat 3/9/19	Fri 4/19/19		
Assemble Complete System	14 days	Sat 3/9/19	Fri 3/22/19		Andrew Cantrell,Timothy Oshatyuk,Slavisa Tosanovic,Evan Von Duhn
Test Complete System	21 days	Sat 3/23/19	Fri 4/12/19	19	Andrew Cantrell,Timothy Oshatyuk,Slavisa Tosanovic,Evan Von Duhn
Revise Complete System	21 days	Sat 3/23/19	Fri 4/12/19	19	Andrew Cantrell,Timothy Oshatyuk,Slavisa Tosanovic,Evan Von Duhn
Demonstration of Complete System	7 days	Sat 4/13/19	Fri 4/19/19	21	Andrew Cantrell,Timothy Oshatyuk,Slavisa Tosanovic,Evan Von Duhn

Develop Final Report	**99 days**	**Mon 1/14/19**	**Mon 4/22/19**		
Write Final Report	99 days	Mon 1/14/19	Mon 4/22/19		Andrew Cantrell,Timothy Oshatyuk,Slavisa Tosanovic,Evan Von Duhn
Submit Final Report	0 days	Mon 4/22/19	Mon 4/22/19	24	Timothy Oshatyuk
Spring Recess	7 days	Mon 3/25/19	Sun 3/31/19		
Project Demonstration and Presentation	0 days	Fri 4/26/19	Fri 4/26/19		Andrew Cantrell,Timothy Oshatyuk,Slavisa Tosanovic,Evan Von Duhn

VI. Design Team Information:

Andrew Cantrell, CPE, ESI(Y), Software Manager

Timothy Oshatyuk, EE, ESI(N), Archivist

Slavisa Tosanovic, EE, ESI(N), Team Leader

Evan Von Duhn, CPE, ESI(Y), Hardware Manager

VII. Conclusions and Recommendations (AC)

The current status of the design includes a multitap transformer power source with eight different voltage rails: ±6 V, ±12 V, ±18 V, ±24 V. These rails will each be capable of switching on and off using a configuration of MOSFETs. The rails will all connect, through diodes, to the same power inputs of an audio amplifier. The diodes will allow whatever rail is active to pass its voltage to the amplifier, while preventing current from traveling backwards to the other rail connections which will be set to low voltage. An analog to digital converter (ADC) will be used to sample an audio signal. A microcontroller, namely a dsPIC33, will be running software to analyze the discrete samples produced by the ADC and determine which rails must be active. Based on the software results, the dsPIC33 will generate signals to each of the MOSFETs,

turning on the needed rail and turning all other rails off. The audio signal samples used by the dsPIC33 will then be converted back to the original analog audio signal through a digital to analog converter (DAC) which is included in the dsPIC33 hardware. The audio signal produced by the DAC will then travel to the amplifier circuit which will already be set to an appropriate voltage rail value.

In order to have a successful design, the dsPIC33 must be configured to receive data from the ADC. The data will be sent via I2C, thus the "config" files of the dsPIC33 must be set to allow for I2C communication. Any final design changes will be applied when building the physical circuit as a result of testing and troubleshooting. The designed amplifier should be able to perform within the design requirements stated previously. During the final semester, the first step will be to begin building the amplifier circuit, the second step will be to test and troubleshoot the circuit to get it in working order, and lastly, some values and/or components may be interchanged in an effort to get better results.

VIII. References:

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[2] Zhang, Xiang, and Liter Siek. "An 80.4% Peak Power Efficiency Adaptive Supply Class H Power Amplifier for Audio Applications." , vol. 25, no. 6, 2017, pp. 1954–1965., doi:10.1109/tvlsi.2017.2666268.

[3] Sedra, Adel S., and Kenneth Carless. Smith. *Microelectronic Circuits*. Oxford University Press, 2004.

[4] Zhivomirov, H., and N. Kostov. "Power Parameters and Efficiency of Class B Audio Amplifiers in Real-World Scenario." *Radioengineering*, vol. 26, no. 1, 2017, pp. 258–262., doi:10.13164/re.2017.0258.

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[8] "US7315204B2 - Class AB-D Audio Power Amplifier." *Google Patents*, Google, patents.google.com/patent/US7315204B2/en.

[9] "What is High-Resolution Audio (HRA) ," *What is High-Resolution Audio (HRA) | High Resolution Audio | Technics US*. [Online]. Available: https://www.technics.com/us/high-res-audio/what-is-high-resolution-audio.html. [Accessed: 10-Oct-2018].

IX. Appendices

A)   MATLAB Code

```matlab
%Andrew Cantrell
%Power/Energy Simulation
clc; format compact; clear all;


Fs = 44100; %Sample frequency = 44.1kHz for quality audio
rail1 = 5;
rail2 = 10;
rail3 = 15;
rail4 = 20;
load = 8;


%choose .wav file: classical, rock, punk, jazz, dance
[audio,Fs] = audioread('classical.wav'); %sample audio file at 44.1kHz
sampleNum = size(audio,1);


for n = 1:sampleNum
    x(n) = abs(audio(n)); %Consider the absolute value of the signal
end


scale = rail4/max(x);
%Scale the signal to its aplified value
for n = 1:sampleNum
    x(n) = x(n)*scale;
end


y(1) = 0; %need initial condition, y(n) depends on y(n-1)
rail = zeros();
rail1samp = 0;
rail2samp = 0;
rail3samp = 0;
rail4samp = 0;


for n = 2:sampleNum
    if(x(n)>=y(n-1)-.001)
        y(n) = x(n);
    else
        y(n)= y(n-1)-.001;
    end
    if(y(n)>=rail3-.3)
        rail(n)=rail4;
        rail4samp = rail4samp+1;
    elseif(y(n)>=rail2-.3)
        rail(n)=rail3;
        rail3samp = rail3samp+1;
```

```
    elseif(y(n)>=rail1-.3)
        rail(n)=rail2;
        rail2samp = rail2samp+1;
    else
        rail(n)=rail1;
        rail1samp = rail1samp+1;
    end
end


DynP =
(rail1samp*(rail1^2)/load)+(rail2samp*(rail2^2)/load)+(rail3samp*(rail3^2)/load)+(rail4samp*(rail4^2)/l
oad);
DynP = DynP/sampleNum;
StdP = (rail4^2)/load
PercentDecrease = ((StdP-DynP)/StdP)*100
Mosfet = DynP + 4*.300
PercentDecrease = ((StdP-Mosfet)/StdP)*100


figure
hold on
plot(rail)
plot(x)
plot(y)
hold off
```

B)   Datasheets

FDG6322C: https://www.mouser.com/datasheet/2/308/FDG6322C-1300406.pdf

Edwards 596: https://edwards-signals.com/files/c-590_Series_Transformers_Catalog_Page.pdf

DM240001-3: http://microchipdeveloper.com/boards:explorer1632

TPA3130D2DAPR: http://www.ti.com/lit/ds/symlink/tpa3130d2.pdf

MA330019: http://ww1.microchip.com/downloads/en/DeviceDoc/70325b.pdf

dsPIC33FJ128GP804: http://ww1.microchip.com/downloads/en/DeviceDoc/70292G.pdf

MB4S-TP: http://www.mccsemi.com/up_pdf/MB05S-MB10S(MBS-1).pdf

TLV320ADC3001: http://www.ti.com/lit/ds/symlink/tlv320adc3001.pdf

BAV19: https://www.mouser.com/ds/2/149/BAV19-888520.pdf